

## AMENDMENTS

### In The Claims

**Claim 1. (currently amended)** An electrostatic discharge (ESD) protection device, comprising:

an ~~ESD clamp circuit~~ ESD protection circuit, comprising:

at least a diode connected in series between a first voltage and a pad; and

at least an ESD component connected in series between a second voltage and a pad,

wherein each of the at least an ESD component comprises a deep N-well region formed in a P-type substrate, a triple P-well formed in the deep N-well region, and a highly doped N-type (N+) region and a highly doped P-type (P+) region formed in the triple P-well region.

**Claim 2. (original)** The ESD protection device of claim 1, wherein when a number of the ESD component is one, the N+ region of the ESD component is connected to the pad, and the P+ region of the ESD component is connected to the second voltage.

**Claim 3. (original)** The ESD protection device of claim 1, wherein when a number of the ESD component is two including a 1<sup>st</sup> ESD component and a 2<sup>nd</sup> ESD component, the N+ region of a 1<sup>st</sup> ESD component is connected to the pad, the P+ region of the 2<sup>nd</sup> ESD component is connected to the second voltage, and the P+ region of the 1<sup>st</sup> ESD component is connected to the N+ region of the 2<sup>nd</sup> ESD component.

**Claim 4. (original)** The ESD protection device of claim 1, wherein when a number of the ESD component is S including a 1<sup>st</sup> ESD component to a S<sup>th</sup> ESD component, the N+ region

of the 1<sup>st</sup> ESD component is connected to the pad, the P+ region of the S<sup>th</sup> ESD component is connected to the second voltage, and the P+ region of the T<sup>th</sup> ESD component is connected to the N+ region of the (T + 1)<sup>th</sup> ESD component, wherein S is a positive integer and T is a positive integer from 1 to S-1.

**Claim 5. (original)** The ESD protection device of claim 1, wherein each of the at least a diode comprises a N-well region formed in a P-type substrate, and a N+ region and a P+ region formed in the N-well region.

**Claim 6. (original)** The ESD protection device of claim 1, wherein when a number of the diode is one, the N+ region of the diode is connected to the first voltage, and the P+ region of the diode is connected to the pad.

**Claim 7. (original)** The ESD protection device of claim 1, wherein when a number of the diode is two including a first diode and a second diode, the N+ region of a first diode is connected to the first voltage, the P+ region of the second diode is connected to the pad, and the P+ region of the first diode is connected to the N+ region of the second diode.

**Claim 8. (original)** The ESD protection device of claim 1, wherein when a number of the diode is S including a 1<sup>st</sup> diode to a S<sup>th</sup> diode, the N+ region of the 1<sup>st</sup> diode is connected to the first voltage, the P+ region of the S<sup>th</sup> diode is connected to the pad, and the P+ region of the T<sup>th</sup> diode is connected to the N+ region of the (T + 1)<sup>th</sup> diode, wherein S is a positive integer and T is a positive integer from 1 to S-1.

**Claim 9. (currently amended)** The of claim 1, wherein the ESD protection ~~circuit~~ device further comprises another ~~ESD clamp circuit~~ ESD protection circuit comprising:

a PMOS transistor; and

an NMOS transistor, wherein a gate of the PMOS transistor and a gate of the NMOS transistor are connected to the pad, a source of the PMOS transistor is connected to a drain of the NMOS transistor, a drain of the PMOS transistor is connected to the first voltage, and a source of the NMOS transistor is connected to the second voltage.

**Claim 10. (original)** The ESD protection device of claim 1, wherein the ESD protection device is a radio frequency (RF) ESD protection device.

**Claim 11. (currently amended)** An electrostatic discharge (ESD) protection device, comprising:

~~an ESD clamp circuit~~ ESD protection circuit, comprising:

at least a first ESD component connected in series between a first voltage and a pad; and

at least a second ESD component connected in series between a second voltage and a pad, wherein each of the at least a first ESD component or the at least a first ESD component comprises a deep N-well region formed in a P-type substrate, a triple P-well formed in the deep N-well region, and a highly doped N-type (N+) region and a highly doped P-type (P+) region formed in the triple P-well region.

**Claim 12. (original)** The ESD protection device of claim 11, wherein when a number of the first ESD component is one, the N+ region of the first ESD component is connected to the pad, and the P+ region of the first ESD component is connected to the second voltage.

**Claim 13. (original)** The ESD protection device of claim 11, wherein when a number of the first ESD component is two including a 1<sup>st</sup> first ESD component and a 2<sup>nd</sup> first ESD component, the N+ region of a 1<sup>st</sup> first ESD component is connected to the pad, the P+ region of the 2<sup>nd</sup> first ESD component is connected to the second voltage, and the P+ region of the 1<sup>st</sup> first ESD component is connected to the N+ region of the 2<sup>nd</sup> first ESD component.

**Claim 14. (original)** The ESD protection device of claim 11, wherein when a number of the first ESD component is S including a 1<sup>st</sup> first ESD component to a S<sup>th</sup> first ESD component, the N+ region of the 1<sup>st</sup> first ESD component is connected to the pad, the P+ region of the S<sup>th</sup> first ESD component is connected to the second voltage, and the P+ region of the T<sup>th</sup> first ESD component is connected to the N+ region of the (T+1)<sup>th</sup> first ESD component, wherein S is a positive integer and T is a positive integer from 1 to S-1.

**Claim 15. (original)** The ESD protection device of claim 11, wherein when a number of the second ESD component is one, the N+ region of the second ESD component is connected to the first voltage, and the P+ region of the second ESD component is connected to the pad.

**Claim 16. (original)** The ESD protection device of claim 11, wherein when a number of the second ESD component is two including a 1<sup>st</sup> second ESD component and a 2<sup>nd</sup> second ESD component, the N+ region of a 1<sup>st</sup> second ESD component is connected to the first voltage,

the P+ region of the 2<sup>nd</sup> second ESD component is connected to the pad, and the P+ region of the 1<sup>st</sup> second ESD component is connected to the N+ region of the 2<sup>nd</sup> second ESD component.

**Claim 17. (original)** The ESD protection device of claim 11, wherein when a number of the second ESD component is S including a 1<sup>st</sup> second ESD component to a S<sup>th</sup> second ESD component, the N+ region of the 1<sup>st</sup> second ESD component is connected to the first voltage, the P+ region of the S<sup>th</sup> second ESD component is connected to the pad, and the P+ region of the T<sup>th</sup> second ESD component is connected to the N+ region of the (T+1)<sup>th</sup> second ESD component, wherein S is a positive integer and T is a positive integer from 1 to S-1.

**Claim 18. (original)** The ESD protection device of claim 11, wherein the ESD protection device is a radio frequency (RF) ESD protection device.

**Claim 19. (currently amended)** The ESD protection device of claim 11, wherein the ESD protection ~~circuit device~~ further comprises another ~~ESD clamp circuit~~ ESD protection circuit comprising:

a PMOS transistor; and

an NMOS transistor, wherein a gate of the PMOS transistor and a gate of the NMOS transistor are connected to the pad, a source of the PMOS transistor is connected to a drain of the NMOS transistor, a drain of the PMOS transistor is connected to the first voltage, and a source of the NMOS transistor is connected to the second voltage.